IN THE CLAIMS

Please cancel Claims 23-24 and 26-30 without prejudice, amend Claims 1, 8, 9, 18, 21 and 25, and add new Claims 31-46 as follows:

1. (Currently Amended) A processor interface device used in an extensible processor, comprising:

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

a data transfer fabric adapted to transfer data and signals between said at least one memory port and said at least one function port, and

an arbitration unit adapted to arbitrate access to various portions of said ~~memory~~ storage device by said macro function.

2. (Previously presented) The processor interface device of Claim 1, wherein said data transfer fabric comprises a crossbar switch fabric.

3. (Previously presented) The processor interface device of Claim 1, further comprising a macro function in data communication with said at least one function port, said macro function being controlled at least in part by a processor instruction associated with said macro function, wherein said macro function may access said at least one memory port.

4. (Previously presented) The processor interface device of Claim 1, further comprising a plurality of macro functions in data communication with respective ones of said function ports, said interface device further adapted to allow simultaneous access of multiple ones of said memory ports by respective ones of said macro functions via said function ports.

5. (Previously presented) The processor interface device of Claim 4, wherein said at least one of said macro functions is controlled by at least one processor instruction associated with an instruction set of a host processor.

6. (Previously presented) The processor interface device of Claim 5, wherein said host processor comprises an extensible RISC processor, and said instruction set comprises an extended instruction set thereof.

7. (Previously presented) The processor interface device of Claim 5, wherein said data transferred from said storage device via said interface device is processed in pipeline fashion by at least two of said plurality of macro functions.

8. (Currently amended) The interface device of Claim 7, wherein said act of processing in pipeline fashion comprises[;] :

assigning each of said at least two macro functions as particular stages in a pipeline; and

sequentially processing said data in said stages of said pipeline.

9. (Currently amended) A user-configured processing device, comprising:

a first data processor having an instruction set associated therewith;

a second data processor adapted to process data in a predetermined manner;

a memory array having at least one memory bank, said at least one memory bank being adapted to store a plurality of data; and

a memory interface, said memory interface having at least one first port adapted for data communication between said interface and said memory array, and at least one second port adapted for data communication between said interface and said second processor;

wherein access to said memory array via said at least one memory port is controlled at least in part by said second data processor; and

wherein at least a portion of said processing device comprises extension hardware selected by said user at time of design of said processing device.

10. (Previously presented) The device of Claim 9, further comprising an arbitration unit which arbitrates access to said at least one memory bank during said access to said memory array.

11. (Previously presented) The device of Claim 9, wherein said at least one function port further comprises at least one function controller having a plurality of registers.

12. (Previously presented) The device of Claim 11, wherein said plurality of registers comprises registers selected from the group comprising control, status, and test registers.

13. (Previously presented) The device of Claim 11, wherein said at least one function controller further comprises an interface to at least one pipeline stage of said first data processor.

14. (Previously presented) The device of Claim 9, further comprising a crossbar adapted for data communication between said at least one memory port and said at least one function port.

15. (Previously presented) The device of Claim 14, wherein said crossbar permits simultaneous access to each of said at least one memory ports by at least one of said at least one function ports.

16. (Previously presented) The device of Claim 9, wherein said second data processor comprises a digital signal processor, said digital signal processor being optimized for calculation based on at least one predetermined algorithm.

17. (Previously presented) The device of Claim 9, wherein said second data processor comprises an application specific integrated circuit (ASIC).

18. (Currently amended) A method of accessing data disposed within ~~a plurality of~~ X and Y memory banks as respective first and second pages, comprising;

providing at least first and second macro functions adapted to process data;

providing a memory interface having at least two function ports and two memory ports, each of said memory ports being in data communication with respective ones of said memory banks, each of said function ports being capable of data communication with each of said memory ports, said first and second macro functions being in data communication with respective ones of said at least two function ports;

controlling the operation of said first and second macro functions using at least one host processor instruction; and

simultaneously accessing said pages of data disposed ~~with in~~ within respective ones of said memory banks using respective ones of said macro functions such that two operand sources are provided simultaneously.

19. (Previously presented) The method of Claim 18, further comprising arbitrating access to said at least two memory ports by said at least first and second function ports using a crossbar.

20. (Previously presented) The method of Claim 18, wherein the act of controlling comprises initiating at least one of said first and second macro functions using an instruction decoded in the instruction decode stage of the host processor.

21. (Currently amended) The method of Claim 20, wherein the act of controlling further comprises controlling at least one of said macro functions based at least in part on one immediate ~~(imm)~~ operand derived from said decoded instruction.

22. (Previously presented) The method of Claim 18, wherein the act of controlling comprises accessing at least one extension register resident within said host processor.

23. -24. (Cancelled)

25. (Currently amended) A processing device, comprising:

first means for processing data, said first means for processing having ~~an~~ a base instruction set and extension instruction set associated therewith;

second means for processing data, said second means being adapted to process data in a predetermined manner;

memory means having at least one memory bank, said at least one memory bank being adapted to store a plurality of data;

interface means, said interface means having at least one first port adapted for data communication between said interface means and said memory means, and at least one second port adapted for data communication between said interface means and said second means for processing;

wherein access to said memory means via said at least one memory port is controlled at least in part by an instruction associated with said extension instruction set of said ~~second~~ first means for processing.

26. - 29. (Cancelled)

30. (Cancelled).

31. (New) A user-configurable processor having a processor interface device associated therewith, comprising:

a processor core in operative communication with said interface device;

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

a data transfer fabric adapted to transfer data and signals between said at least one memory port and said at least one function port, and

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function;

wherein at least a portion of said interface comprises extension hardware selectively added by said user at time of said configuration.

32. (New) The processor of Claim 31, further comprising a macro function in data communication with said at least one function port, said macro function being controlled at least in part by a processor extension instruction associated with said macro function, wherein said macro function may access said at least one memory port, said extension instruction being selected by said user at said time of configuration.

33. (New) The processor interface device of Claim 31, further comprising a plurality of macro functions in data communication with respective ones of said function ports, said interface device further adapted to allow simultaneous access of multiple ones of said memory ports by respective ones of said macro functions via said function ports.

34. (New) The processor interface device of Claim 33, wherein said at least one of said macro functions is controlled by at least one processor instruction associated with an instruction set of a host processor.

35. (New) The processor interface device of Claim 34, wherein said data transferred from said storage device via said interface device is processed in pipeline fashion by at least two of said plurality of macro functions.

36. (New) The interface device of Claim 35, wherein said act of processing in pipeline fashion comprises:

assigning each of said at least two macro functions as particular stages in a pipeline; and

sequentially processing said data in said stages of said pipeline.

37. (New) A user-configurable processor device having a standardized processor interface device and configurable DSP core associated therewith, comprising:

a processor core in operative communication with said interface device;

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

a data transfer fabric adapted to transfer data and signals between said at least one memory port and said at least one function port, and

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function;

wherein at least a portion of said interface comprises extension hardware selectively added by said user at time of said configuration; and

wherein said standardized interface is adapted to interface with any of a plurality of different configurations of said DSP core selected by said user at said time.

38. (New) The processor device of Claim 37, further comprising an software wrapper associated with said DSP to translate at least some signals exchanged between said DSP core and said standardized interface.

39. (New) The processor device of Claim 38, wherein said software wrapper comprises an HDL wrapper, said HDL wrapper being configured at least in part at said time.

40. (New) A user-configurable processor having a standardized processor interface device and user-configurable DSP core associated therewith, comprising:

a RISC core in operative communication with said interface device;

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

a data transfer fabric adapted to transfer data and signals between said at least one memory port and said at least one function port, and

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function;

wherein said standardized interface is adapted to interface with any of a plurality of different configurations of said DSP core selected by said user at the time of said user-configuration.

41. (New) A user-configurable processing device having a user-configured processor

interface device and DSP core associated therewith, comprising:

a RISC core in operative communication with said interface device;

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

a data transfer fabric adapted to transfer data and signals between said at least one memory port and said at least one function port, and

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function;

wherein said DSP core is specifically configured by said user to inter-operate with said interface.

42. (New) A processor device having a processor interface device associated therewith, comprising:

a processor core in operative communication with said interface device;

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

at least one function controller operatively coupled to said at least one function port, said controller being adapted to control at least one aspect of the operation of said at least one port;

a data transfer fabric adapted to transfer data and signals between said at least one memory port and said at least one function port,

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function;

43. (New) A user-configurable processing device having a first processor core, a user-configured processor interface device, and second core associated therewith, the interface comprising:

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port and associated function controller, said at least one function port and controller cooperating to transfer data and signals to and from a macro function;

a data transfer medium adapted to transfer data and signals between said at least one memory port and said at least one function port, and

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function;

wherein said second processor core is specifically configured by said user at time of design to inter-operate with said interface.

44. (New) An processing device, comprising:

at least one extended processor core, said processor core having both base and extension instruction sets;

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

a macro function in data communication with said at least one function port, said macro function being controlled at least in part by a user-selected instruction within said extension instruction set, wherein said macro function may access said at least one memory port;

a data transfer apparatus adapted to transfer data and signals between said at least one memory port and said at least one function port, and

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function.

45. The processing device of Claim 44, wherein said processor core, memory port, function port, macro function, data transfer apparatus and arbitration unit are all disposed on a single die.

46. Data processing apparatus, comprising:

an extended RISC processor core having base and extension instruction sets;

a memory interface;

a signal processing macro function optimized to perform a particular processing algorithm;

an XY memory array; and

an I/O interface;

wherein said RISC processor core and said macro function are coupled such that said macro function and said memory interface substantially comprise at least a portion of RISC processor's instruction set, said macro function being controlled at least in part by decoded instructions generated by the pipeline decode stage of the RISC processor; and

wherein one or more peripheral devices operatively coupled to said I/O interface are provided direct memory access (DMA) capability to said XY memory array.